High Speed Hardware Architectures
Handlungsfeldkonferenz zur optischen Kommunikationstechnik
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Outline – 3D Integration

- 3D Integration - Introduction
- Optical Sensor Array
- 3D Hybrid Integration
- 3D Roadmap
3D Integration – Motivation

Intel’s 3D-TSV prototype

Author’s conclusion [2]:
- EDA challenge
- Signal / Power Integrity
- Signaling (chip-to-chip)

- Novel sensor platform for bioanalytics
- Goal: Proof-Of-Concept demonstrator for the detection of Staphylococcus aureus (SA) germs
- Sensor platform will incorporate optical microresonators achieving a high specificity
- Appliance of modulation technique for individual analysis of the activation of diverse antibody/antigen reactions via evanescent field sensing
- HS Deliverables SiN-test chips, characterisation and analysis

160 (SiN)-Mikroringe auf 2 cm²
(11 250 Chips auf 8 Zoll)
(SOI: 0,5 mm²/Chip
⇒ 45 000 Chips auf 8 Zoll)

⇒ adaptierbar auf Nachweis unterschiedlicher Spezies
Application – Optical Sensor

Sensor Array for Multiparameter Detection
Miniaturised multisensor platform for online label-free optical biomolecule detection

4” wafer – 12 cascaded microring elements

Multi-contact probehead

reference-microring
Sensor Array

- fluidic cell required for well-controlled and reproducible analyte flow
- Construction and implementation of a fluidic cell made of PDMS

- optical coupling via grating couplers

source: helios-project.eu
Explosives Detection - Results

- Actual detection limit: 0.5 ppb
- Expected detection limit <0.1 ppb

R. Orghici et al., A Microring Resonator Sensor for Sensitive Detection of 1,3,5-Trinitrotoluene (TNT), Sensors 10 (2010) 6788
Sensor Array w/ 12 Microrings - Results

Individual identification of μrings by complete parallel modulation and detection
Challenge hybrid 3D Integration

High Speed Hardware Architecture

Connection diagram showing:
- Sensor Array
- Electronic
- Package
- TSVs
- System I/O

Key connections:
- PWR
- GND
- CLK
Electro-Optic Smart-System

- Step 1: Chip on Chip / FlipChip
  - Digital interface on-chip
  - Programmable frequency synthesizer (microring modulation) on-chip

- Step 2: Electro-optic system on-chip
  - CMOS integration electronics and optics
  - Omission of interconnect technology
  - Electro-optic microring modulation

- Step 3: Full integration incl. detector and laser
Perspective: Electronic Front-End

Smart sensor microsystem front-end

I/O module
- Sensor interfacing
- Modulation interface
- Laser

Smart sensor control unit
- Data acquisition module
- Realtime calibration
- Microring labeling control unit
- Laser interface
- Laser modulation
- Measurement controller

User interface (GUI/MMI)
I/O Chip-to-Chip target:
→ I/O + repeater in loop forward architecture
→ 25 Gbps/pin @ 200 mVpp
→ 8 Gbps /pin / 25mVpp

Research:
Universität Stuttgart
Institut für Elektrische und Optische Nachrichtentechnik
Lehrstuhl Prof. Dr. Berroth / Dipl.-Ing. Johannes Reichart
Author’s recommendation [1]:
• 3D Si integration is a long way to go. A lot of R & D topics.
• Industry should build ecosystem incorporating standards and infrastructure so that EDA vendors can create and qualify the software for design.
• Passive or active interposers technologies are the key for mass products
• ……..

Author’s conclusion [2]:
• There are still no microelectronic products based on 3D TSV technologies in the market – except CMOS image sensors.
• 3D technology platform further developments are focusing on the robustness of the fabrication processes and especially on reliability issues of advanced 3D integrated heterogeneous systems for future applications.

3D Integration = Key Technology!

- 3D Integration research areas of interest:
  - chip-to-chip interconnect technologies
  - Design for testability
  - EDA challenge

- Application
  - biosensor technology
  - optical network technology
  - ........
Thanks for your attention!

HHI - Leading Research Institute for Mobile and Fixed Communications Networks
Characterization of RF Power Amplifiers

- Precise characterization for modulated signals
- Identification of memory effects (amplitude and phase)

Digital Pre-distortion

- Development of a measurement setup for very precise memoryless predistortion
- Temperature independent predistortion system

Design of CMOS Power Amplifier

- Development of scalable models for L,C,R parasitics of huge transistor arrays
- Development of BGA CMOS power amplifier for GSM
- Measurement and load optimization of fabricated CMOS PAs

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Internal and External Collaboration

- **Industrial**
  - Vistec
  - FAB
  - LG
  - Nokia Siemens Networks
  - CU TEC
  - MAZ
  - Micram
  - Melexis
  - Infineon
  - The MathWorks
  - PANalytical
  - WINCOR NIXDORF
  - Swissbit
  - alpha-board
  - GLOBALFOUNDRIES
  - ARRI

- **FhG, HHI / Institutes**
  - Fraunhofer
  - CASED
  - IHP
  - IMMS

- **Universities**
  - Freie Universität Berlin
  - Technische Universität Berlin
  - TU Berlin
  - HTW Berlin
  - Universität Darmstadt
  - Universität Heidelberg
  - Universität Stuttgart
  - TU Clausthal
  - Universität Wien

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